	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	45037	((top or second) adj2 (electrodes or electrode))	USPAT	2002/03/29 10:32
2	BRS	L2	3528	1 same (heat or heating or annealing or anneal or rapid)	USPAT	2002/03/29 10:36
3	BRS	L3	723	2 same (before or after)	USPAT	2002/03/29 10:37
4	BRS	L4	95	3 same (ferroelectric or pzt)	USPAT	2002/03/29 10:37
5	BRS	L5	42639	((bottom or first) adj2 (electrodes or electrode))	USPAT	2002/03/29 10:39
6	BRS	L6	53	4 same 5	USPAT	2002/03/29 10:39

DOCUMENT-IDENTIFIER: US 6322849 B1
TITLE: Recovery of electronic properties in hydrogen-damaged ferroelectrics by
low-temperature annealing in an inert gas

---------- KWIC ---------

DEPR:
The switch is typically a MOSFET. In step 416, an insulating layer is formed to separate the switching element from the **ferroelectric** element to be formed.
In step 418, a **bottom electrode** is formed. Preferably, the electrode is made
of platinum and is sputter-deposited to form a layer with a thickness of about
2000 .ANG.. In the preferred method, an adhesion layer made of titanium or
titanium nitride of about 200 .ANG. would be formed in this step prior to depositing the electrode. The **ferroelectric** thin film is applied to the **bottom**
electrode in step 422. In the preferred method, the **ferroelectric** thin film contains layered superlattice material. An MOCVD method is the most preferred
method to form the thin film. The **ferroelectric** thin films also can be applied
using a liquid deposition technique, such as a spin-coating or a misted deposition method as described in U.S. Pat. No. 5,456,945. In step 420, chemical precursors of the layered superlattice material that will form the desired **ferroelectric** thin film are prepared. Usually, precursor solutions are
prepared from commercially available solutions containing the chemical precursor compounds. A preferred embodiment utilizes a precursor solution containing relative molar proportions of the elements strontium, bismuth,

and
tantalum corresponding approximately to the formula SrBi.sub.2 Ta.sub.2 O.sub.9. An alternative preferred embodiment utilizes a precursor solution containing relative molar proportions of the elements strontium, bismuth, tantalum and niobium corresponding approximately to the formula SrBi.sub.2 (Ta.sub.1-x Nb.sub.x).sub.2 O.sub.9, where x is about 0.5. Preferably, the concentrations of the various precursors supplied in the commercial solutions
are adjusted in step 420 to accommodate particular manufacturing or operating
conditions. For example, the stoichiometric amounts of the various elements in
a commercial solution for a layered superlattice thin film might be SrBi.sub.2.18 (Ta.sub.1.44 Nb.sub.0.56)O.sub.9. It might be desirable, however, to add extra niobium or bismuth to this solution to generate extra oxides that will protect the **ferroelectric** compounds from hydrogen-**annealing**
degradation. The application step 422 is preferably followed by a treatment step 424, which preferably includes a drying step in case of liquid deposition,
a crystallization substep at elevated temperatures such as a **rapid** thermal process (RTP), and may include treatment with ultraviolet radiation during or **after** the application step 422. For example, in a typical spin-on procedure, a
coat of the precursor might be applied and dried. Then another precursor coat
might be applied and dried. The application and treatment steps 422 and 424
can be repeated several times. The treated film is then annealed in oxygen to
form the resulting **ferroelectric** thin film in step 426. Following steps 422-426, the **top electrode** is formed in step 428. Step 428 and other steps
typically include high-energy material deposition and patterning substeps, such
as target sputtering, ion milling or RIE-etching, and ashing.

DOCUMENT-IDENTIFIER: US 6281023 B1
TITLE: Completely encapsulated top electrode of a ferroelectric capacitor using
a lead-enhanced encapsulation layer

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DEPR:
In FIG. 8, contact holes are etched to provide access of the **top and bottom electrodes** 22 and 18. Contact hole 32 provides access to **bottom electrode** 18,
and contact holes 34 provide access to **top electrodes** 22. Contact holes 34 are
etched through the dielectric layer 24 and the second **ferroelectric** layer 30 to
allow metalization of the **top electrodes**. Contact hole 32 is etched through the dielectric layer 24 and the first **ferroelectric** layer 20 to allow
metalization of **bottom electrode** 18. Note that the contact holes 32 and 34 are
ideally etched in two steps. The first etching step removes the dielectric layer 24 in the contact holes. The dielectric oxide material can be etched away using a fluorine-based wet or dry etch. It is desirable that a sloped profile is etched into the contact holes. **After** the dielectric oxide material is removed, the remaining **ferroelectric** material in the contact hole is etched
away according to the **ferroelectric** etch described above. Note in FIG. 8 that
contact holes 32 and 34 are etched through about the same thickness of material, i.e. 5000 Angstroms of glass plus 3000 Angstroms of **ferroelectric** material. Therefore, the etching of contact holes 32 and 34 can be performed
simultaneously. **After** contact holes 32 and 34 are etched, an optional second

recovery **anneal** can be performed. The optional second recovery **anneal** includes
a 550.degree. C. **heat** treatment for about sixty minutes in an oxygen atmosphere.

DEPR:
FIG. 11 is the same sectional view as FIG. 3, showing the sequential deposition
of a thick glass layer 16, a **bottom electrode** layer 18, a first **ferroelectric** layer 20, and a **top electrode** layer 22. All of the thicknesses and materials described above are the same in FIG. 11. A first **anneal** can be performed **after**
the first **ferroelectric** layer 18 is deposited. The platinum **top electrode** layer 22 is etched to form individual **top electrodes** 22. A second **anneal** can
be performed **after the top electrodes** 22 are etched.

DEPR:
In FIG. 12, the first **ferroelectric** layer 20 is etched with some lateral overlap of the etched **top electrodes** 22. The **bottom electrode** layer 18 is etched to define the dimensions of a **bottom electrode**. As can be seen in FIG.
12, one end of the **bottom electrode** 18 is etched to allow sufficient room for
the eventual **bottom electrode** contact. The other end of **bottom electrode** 18 is
etched to the same dimensions as the first **ferroelectric** layer 20. The etching
techniques for **bottom electrode** 18 and first **ferroelectric** layer 20 are as described above with reference to FIGS. 3-11. **After** the first **ferroelectric**
layer 20 and **bottom electrode** layer 18 are etched, an optional first recovery
anneal can be performed. The optional first recovery **anneal** includes a 550.degree. C. **heat** treatment for about sixty minutes in an oxygen atmosphere.

DEPR:
In FIG. 16, contact holes are etched to provide access of the **top and bottom electrodes** 22 and 18. Contact hole 32 provides access to **bottom electrode** 18, and contact holes 34 provide access to **top electrodes** 22. Note that in FIG. 16, both contact holes 34 and 32 are etched through the dielectric layer 24 and the second **ferroelectric** layer 30 to allow metalization of the **top and bottom electrodes**. The thickness of contact holes 34 and 32 is the same since they are etched through the same thickness of material. Contact holes 32 and 34 are ideally simultaneously etched in two steps to remove the dielectric oxide material and then the remaining **ferroelectric** material. The type of etch used in the same as described with reference to FIG. 8. **After** contact holes 32 and 34 are etched, an optional second recovery **anneal** can be performed.

DEPR:
FIGS. 19-21 are identical to previously described FIGS. 11-13 both in sectional views, material, etching, and **annealing** steps. FIG. 19 shows a thick glass layer 16, a **bottom electrode** layer 18, a first **ferroelectric** layer 20, and a **top electrode** layer 22 formed in sequence, wherein the **top electrode** layer 22 is etched to form individual **top electrodes** 22. FIG. 20 shows the etching of the first **ferroelectric** layer 20 and the etching of the **bottom electrode** layer 18 to form a **bottom electrode**. In FIG. 21, a second "cap" **ferroelectric** layer 30 about the same thickness (3000 Angstroms) as the first **ferroelectric** layer

20 is deposited over the first **ferro lectric** layer 20, thereby completely encapsulating the **top l ctrod s** 22. A first **anneal** is performed **aft r th f rro lectric** layer 20 is deposited, a second **ann al** is performed **aft r th top**
electrode layer 22 is etched, and an optional third **anneal** is performed **after**
the second **ferroelectric** layer 30 is deposited. A optional first recovery **anneal** is performed **after** the first **ferroelectric** layer 20 and **bottom electrode**
layer 18 have been etched.

DEPR:
In FIG. 23, contact holes are etched to provide access of the **top and bottom**
electrodes 22 and 18. Contact hole 32 provides access to **bottom electrode** 18,
and contact holes 34 provide access to **top electrodes** 22. Note that in FIG. 23, both contact holes 34 and 36 are etched through the dielectric layer 24 and
the second **ferroelectric** layer 30 to allow metalization of the **top and bottom**
electrodes. The thickness of contact holes 34 and 32 is the same since they are etched through the same thickness of material. Contact holes 32 and 34 are
ideally simultaneously etched in two steps to remove the dielectric oxide material and then the remaining **ferroelectric** material. The type of etch used
in the same as described with reference to FIG. 8. A second optional recovery
anneal can be performed **after** contact holes 32 and 34 have been opened.

DEPR:
In FIG. 27, only the first **ferroelectric** layer 20 is etched to a reasonable overlap of the etched **top electrodes** 22. The **bottom electrode** layer 18 remains
unetched in FIG. 27. An optional first recovery **anneal** is performed **after**

the
first **f rro l ctric** layer 20 is etched.

DEPR:
In FIG. 31, contact holes are etched to provide access of the **top and bottom**
electrodes 22 and 18. Contact hole 32 provides access to **bottom electrode** 18,
and contact holes 34 provide access to **top electrodes** 22. Note that in FIG. 31, both contact holes 34 and 32 are etched through the dielectric layer 24 and
the second **ferroelectric** layer 30' to allow metalization of the **top and bottom**
electrodes. The thickness of contact holes 34 and 32 is the same since they are etched through the same thickness of material. Contact holes 32 and 34 are
ideally simultaneously etched in two steps to remove the dielectric oxide material and then the remaining **ferroelectric** material. The type of etch used
in the same as described with reference to FIG. 8. **After** contact holes 32 and
34 have been etched, an optional third recovery **anneal** can be performed.

DOCUMENT-IDENTIFIER: US 6236076 B1
TITLE: Ferroelectric field effect transistors for nonvolatile memory applications having functional gradient material

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DEPR:
The final precursor solution was applied onto the substrate using a spin-on technique. Two liquid coatings were applied to the samples. Just prior to use, the final liquid precursor was diluted to 0.1 molar concentration by adding n-butyl acetate. A first spincoat of 0.1 molar solution of the final precursor was deposited on **bottom electrode** 318 at 1100 rpm for 40 seconds.
This was dried for one minute at 160.degree. C., and at 260.degree. C. for four minutes. The first spincoat annealed at 800.degree. C. for 10 minutes with an oxygen flowrate of 5 liters/minute, with 10 minutes "push" and 10 minutes "pull". This sequence of the spin-coating and drying was repeated for
a second spincoat. **After** drying the second spin-coat, the wafer was annealed
at 800.degree. C. for 60 minutes with an oxygen flowrate of 5 liters/minute,
with 10 minutes "push" and 10 minutes "pull". Platinum was sputter-deposited
to make **top electrode** layer 322 with 200 nm thickness. The platinum and **ferroelectric** thin film layers were ion-milled to form the capacitors, and then
ashing was performed, followed by a second O.sub.2 **anneal** for 30 minutes at
800.degree. C. The capacitors were patterned so that the MFM capacitors had
surface areas, AMFM, of 4301 and 6940 square microns.

DOCUMENT-IDENTIFIER: US 6204158 B1
TITLE: Reduced diffusion of a mobile specie from a metal oxide ceramic into the
substrate

---------- KWIC ---------

DEPR:
An **anneal** is performed to grown the grains of the metal oxide ceramic in order
to obtain the desired electrical characteristics. The **anneal** also causes the excess mobile to diffuse out and react with the scavenger layer. **After the anneal,** the scavenger and metal oxide ceramic layers are patterned to cover the
bottom electrode. A conductive layer 457 is then deposited over the scavenger
layer to form the **top electrode**. Another **anneal** can be performed **after** formation of the **top electrode** to ensure that a well-defined metal oxide ceramic/electrode interface. The **anneal** to ensure the well-defined interface
can be combined with the **anneal** to achieve good electrical characteristics. Additional processing is performed to complete the **ferroelectric** memory IC.

DOCUMENT-IDENTIFIER: US 6211542 B1
TITLE: Completely encapsulated top electrode of a ferroelectric capacitor using a lead-enhanced escapsulation layer

Inert gas
He, Ne, Ar, Kr, Xe, Rn
Helium Neon Argon Krypton Xenon Radon

---------- KWIC ---------

DEPR:
In FIG. 8, contact holes are etched to provide access of the **top and bottom electrodes** 22 and 18. Contact hole 32 provides access to **bottom electrode** 18, and contact holes 34 provide access to **top electrodes** 22. Contact holes 34 are etched through the dielectric layer 24 and the second **ferroelectric** layer 30 to allow metalization of the **top electrodes**. Contact hole 32 is etched through the dielectric layer 24 and the first **ferroelectric** layer 20 to allow metalization of **bottom electrode** 18. Note that the contact holes 32 and 34 are ideally etched in two steps. The first etching step removes the dielectric layer 24 in the contact holes. The dielectric oxide material can be etched away using a fluorine-based wet or dry etch. It is desirable that a sloped profile is etched into the contact holes. **After** the dielectric oxide material is removed, the remaining **ferroelectric** material in the contact hole is etched away according to the **ferroelectric** etch described above. Note in FIG. 8 that contact holes 32 and 34 are etched through about the same thickness of material, i.e. 5000 Angstroms of glass plus 3000 Angstroms of **ferroelectric** material. Therefore, the etching of contact holes 32 and 34 can be performed simultaneously. **After** contact holes 32 and 34 are etched, an optional second recovery **anneal** can be performed. The optional second recovery **anneal** includes

a 550.degree. C. heat treatment for about sixty minutes in an oxygen
atmosphere.

DEPR:
FIG. 11 is the same sectional view as FIG. 3, showing the sequential deposition
of a thick glass layer 16, a bottom electrode layer 18, a first ferroelectric
layer 20, and a top electrode layer 22. All of the thicknesses and materials
described above are the same in FIG. 11. A first anneal can be performed after
the first ferroelectric layer 18 is deposited. The platinum top electrode
layer 22 is etched to form individual top electrodes 22. A second anneal can
be performed after the top electrodes 22 are etched.

DEPR:
In FIG. 12, the first ferroelectric layer 20 is etched with some lateral
overlap of the etched top electrodes 20. The bottom electrode layer 18 is
etched to define the dimensions of a bottom electrode. As can be seen in FIG.
12, one end of the bottom electrode 18 is etched to allow sufficient room for
the eventual bottom electrode contact. The other end of bottom electrode 18 is
etched to the same dimensions as the first ferroelectric layer 20. The etching
techniques for bottom electrode 18 and first ferroelectric layer 20 are as
described above with reference to FIGS. 3-11. After the first ferroelectric
layer 20 and bottom electrode layer 18 are etched, an optional first recovery
anneal can be performed. The optional first recovery anneal includes a
550.degree. C. heat treatment for about sixty minutes in an oxygen atmosphere.

DEPR:
In FIG. 16, contact holes are etched to provide access of the top and bottom

electrodes 22 and 18. Contact hole 32 provides access to bottom electrode 18, and contact holes 34 provide access to top electrodes 22. Note that in FIG. 16, both contact holes 34 and 36 are etched through the dielectric layer 24 and the second ferroelectric layer 30 to allow metalization of the top and bottom electrodes. The thickness of contact holes 34 and 36 is the same since they are etched through the same thickness of material. Contact holes 32 and 34 are ideally simultaneously etched in two steps to remove the dielectric oxide material and then the remaining ferroelectric material. The type of etch used in the same as described with reference to FIG. 8. After contact holes 32 and 34 are etched, an optional second recovery anneal can be performed.

DEPR:
FIGS. 19-21 are identical to previously described FIGS. 11-13 both in sectional views, material, etching, and annealing steps. FIG. 19 shows a thick glass layer 16, a bottom electrode layer 18, a first ferroelectric layer 20, and a top electrode layer 22 formed in sequence, wherein the top electrode layer 22 is etched to form individual top electrodes 22. FIG. 20 shows the etching of the first ferroelectric layer 20 and the etching of the bottom electrode layer 18 to form a bottom electrode. In FIG. 21, a second "cap" ferroelectric layer 30 about the same thickness (3000 Angstroms) as the first ferroelectric layer 20 is deposited over the first ferroelectric layer 20, thereby completely encapsulating the top electrodes 22. A first anneal is performed after the ferroelectric layer 20 is deposited, a second anneal is performed after the top electrode layer 22 is etched, and an optional third anneal is performed after

the second **ferroelectric** layer 30 is deposited. A optional first recovery **anneal** is performed **after** the first **ferroelectric** layer 20 and **bottom electrode** layer 18 have been etched.

DEPR:
In FIG. 23, contact holes are etched to provide access of the **top and bottom electrodes** 22 and 18. Contact hole 32 provides access to **bottom electrode** 18, and contact holes 34 provide access to **top electrodes** 22. Note that in FIG. 23, both contact holes 34 and 36 are etched through the dielectric layer 24 and the second **ferroelectric** layer 30 to allow metalization of the **top and bottom electrodes**. The thickness of contact holes 34 and 36 is the same since they are etched through the same thickness of material. Contact holes 32 and 34 are ideally simultaneously etched in two steps to remove the dielectric oxide material and then the remaining **ferroelectric** material. The type of etch used in the same as described with reference to FIG. 8. A second optional recovery **anneal** can be performed **after** contact holes 32 and 34 have been opened.

DEPR:
In FIG. 27, only the first **ferroelectric** layer 20 is etched to a reasonable overlap of the etched **top electrodes** 22. The **bottom electrode** layer 18 remains unetched in FIG. 27. An optional first recovery **anneal** is performed **after** the first **ferroelectric** layer 20 is etched.

DEPR:
In FIG. 31, contact holes are etched to provide access of the **top and bottom electrodes** 22 and 18. Contact hole 32 provides access to **bottom electrode** 18, and contact holes 34 provide access to **top electrodes** 22. Note that in FIG. 31, both contact holes 34 and 36 are etched through the

dielectric layer 24 and
the second ferroelectric layer 30' to allow metalization of
the top and bottom
electrodes. The thickness of contact holes 34 and 36 is
the same since they
are etched through the same thickness of material. Contact
holes 32 and 34 are
ideally simultaneously etched in two steps to remove the
dielectric oxide
material and then the remaining ferroelectric material.
The type of etch used
in the same as described with reference to FIG. 8. After
contact holes 32 and
34 have been etched, an optional third recovery anneal can
be performed.

DOCUMENT-IDENTIFIER: US 5466629 A
TITLE: Process for fabricating ferroelectric integrated circuit

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DEPR:
FIG. 6 shows the wafer 10 **after** formation of the **ferroelectric** cell layer 20 and the **top electrode** 14B. The **ferroelectric** layer 20 is preferably made of lead zirconate titanate (**PZT**) deposited on the **bottom electrode** 14A by Sol-Gel spin coating, or MOCVD (metal organic chemical vapor deposition). Sputtering may also be used, however the spin coating and MOCVD tend to fill in the holes, such as 26 better, and thus yield more planar coatings, which are preferable. **After** deposition of the **ferroelectric** thin film, the wafer is oxygen annealed at high temperature to obtain proper remanent polarization and other characteristics. The **annealing** temperature must be compatible with the materials chosen for the contact 36, the barrier layer 22, and the **bottom electrode** 14A. With the materials indicated above, an **annealing** temperature between 550 degrees C. and 650 degrees C. is preferable. The wafer may then be planarized by any of several known planarization methods, though generally it is not made perfectly flat. The **top electrode** 14B, preferably made of platinum, is then formed, preferably by DC magnetron sputtering or RF sputtering. Gold or silver or any conductive material that will resist oxidation may also be used as the **top electrode**. A single photo-mask and etch process, preferably using an RIE of ion-milling etc process, then patterns the **ferroelectric** capacitor 14 and barrier layer 22. In the

embodiment shown in
FIG. 7, the capacitor is shown to partially overlie the transistor 12 and
extend over a substantial portion of the field oxide 34, which provides
sufficient capacitance. Preferably, it overlies the gate 12A of transistor 12
by 10% to 50%. However, it may be larger or smaller depending on the
application, the **ferroelectric** material used, etc. It may extend over as large
an area as conventional stacked capacitors or be limited to a small area on
either side of the hole 26. It is noted that in the region of the contact hole
26, the structure may make little or no contribution to the **ferroelectric**
capacitance because the thickness of the ferromagnetic material 20 is greater
than the other areas. However, this does not degrade the total **ferroelectric**
capacitance severely, since in the structure disclosed there is more than
adequate area for a **ferroelectric** capacitor. Further, since the portion in
contact area 26 acts as a parallel capacitor, it provides some advantages,
namely the elimination of leakage current and the reduction of the possibility
of dielectric breakdown. The invention can also be implemented with many other
ferroelectric materials other than **PZT**. For example, the **ferroelectric**
materials described in U.S. patent application Ser. No. 807,439, which is
hereby incorporated by reference, will also work well with the invention.

DEPR:
FIG. 19 is an embodiment of the invention in which both the **bottom electrode**
151 and the **top electrode** 155 of **ferroelectric** capacitor 150 are made of a
silicon-based material 152, optionally having a thin oxide coating 154. In
this embodiment a layer of conductive silicon-based material 152 is formed in
contact with the contact area 153 of active area 160. The

material 152 is
preferably polysilicon, a silicide, preferably a metal
silicide, or polycide.
The **ferroelectric** layer 156 is formed directly on the
silicon-based layer 152.
During oxygen **annealing**, an oxide coating 154 may form
between the
silicon-based layer 152 and the **ferroelectric** layer 156 to
complete the **bottom**
electrode 151. The **top electrode** 155 may be formed **before**
or after oxygen
annealing, preferably afterwards. The layer 157 is also a
silicon-based
material, preferably polysilicon, a silicide, preferably a
metal silicide, or
polycide. Again an oxide coating 158 may form during the
annealing process.
The oxide coatings 154, 158 should be 5 nm or less thick,
otherwise a parasitic
capacitor may be formed that would divide the voltage
applied to the capacitor
150 and degrade performance. Other materials and processes
in this embodiment
are as discussed in relation to FIGS. 11-13.

DOCUMENT-IDENTIFIER: US 5962069 A
TITLE: Process for fabricating layered superlattice materials and AB0.sub.3 type metal oxides without exposure to oxygen at high temperatures

---------- KWIC ---------

BSPR:
The invention provides a method of fabricating a material selected from the group consisting of layered superlattice compounds and ABO.sub.3 type metal oxide compounds, the method comprising: providing a substrate, and a precursor containing metal moieties in effective amounts for spontaneously forming one of the materials upon **heating** the precursor; applying the precursor to the substrate to form a precursor film; and **heating** the precursor film in an oxygen-free atmosphere at a temperature of between 600.degree. C. and 900.degree. C. to form a solid thin film of the metal oxide on the substrate.
Preferably, the step of **heating comprises rapid** thermal processing the precursor at a temperature of between 500.degree. C. and 850.degree. C.
Preferably, the atmosphere comprises nitrogen, the **rapid** thermal processing temperature is about 650.degree. C., and the **rapid** thermal processing is done for about 30 seconds. Preferably, the step of **heating comprises annealing** in an inert atmosphere at between about 700.degree. C. and 900.degree. C.
Preferably, the step of **annealing comprises annealing** at a temperature of about 800.degree. C. in a nitrogen atmosphere for about thirty minutes. Preferably, the substrate comprises a **first electrode,** and the method further comprises the steps of forming a **second electrode** on the metal oxide,

after the step of
annealing, to form a capacitor, and subsequently performing
a second anneal in
an oxygen-free atmosphere at a temperature of between
300.degree. C. and
900.degree. C. Preferably, the second anneal temperature
is about 800.degree.
C. and is in a nitrogen atmosphere. Alternatively, the
second anneal is in
oxygen at 600.degree. C. Preferably, the metal oxide
comprises a layered
superlattice material, and most preferably, strontium
bismuth tantalate.
Preferably, the method further includes the step of rapid
thermal processing
the precursor film in an atmosphere including oxygen at a
temperature of from
200.degree. C. up to 500.degree. C. Preferably, the
method also includes the
step of drying the precursor film in air at a temperature
of between
140.degree. C. and 320.degree. C. Preferably, the
material forms a portion of
an integrated circuit memory. Preferably the memory is a
memory selected from
the group consisting of DRAMs and ferroelectric FETs.

BSPR:
In another aspect the invention provides a method of
fabricating a metal oxide
selected from the group comprising layered superlattice
compounds and ABO.sub.3
type compounds: providing a substrate, and a precursor
containing metal
moieties in effective amounts for spontaneously forming one
of the metal oxides
upon heating the precursor; applying the precursor to the
substrate; drying the
precursor to form a solid thin film; and heating the solid
thin film on the
substrate without exposing it to oxygen while at a
temperature of 600.degree.
C. or higher to form the material on the substrate.
Preferably, the step of
heating comprises rapid thermal processing the solid thin
film at a temperature
of between 500.degree. C. and 850.degree. C. Preferably,

the step of **heating**
also comprises annealing the solid thin film at a temperature of from
700.degree. C. to 900.degree. C. Preferably, the substrate comprises a **first**
electrode, and the method further comprises the steps of forming a **second**
electrode on the material **after** the step of **annealing**, to form a capacitor, and
subsequently performing a second **anneal** in an oxygen-free atmosphere at a
temperature of between 300.degree. C. and 900.degree. C. Preferably, the
material forms a portion of an integrated circuit memory. Preferably the
memory is a memory selected from the group consisting of DRAMs and
ferroelectric FETs.

DOCUMENT-IDENTIFIER: US 6190926 B1
TITLE: Yield enhancement technique for integrated circuit processing to reduce
effects of undesired dielectric moisture retention and subsequent hydrogen
out-diffusion

---------- KWIC ---------

DEPR:
With reference additionally now to FIG. 1B, the integrated circuit 10 of FIG.
1A is shown **after** undergoing subsequent processing steps as will be more fully
described hereinafter. The integrated circuit 10 is first subject to a **top**
electrode photolithographic operation to remove selected portions of the
structure shown in the preceding figure, followed by a **top** **electrode** etching
and cleaning step. Thereafter, a second **annealing** operation is conducted and a
subsequent **ferroelectric** photolithographic operation is performed to define the
capacitor structure followed by a **PZT** etch and clean operation. At this point,
the **bottom electrode** photolithographic operation is conducted to define the
lower plate of the capacitor followed by a subsequent **bottom electrode** etching
and cleaning step.